4.3 A 400nW Single-Inductor Dual-Input-Tri-Output DC-DC Buck-Boost Converter with Maximum Power Point Tracking for Indoor Photovoltaic Energy Harvesting

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Energy harvesting enables the remote sensors of the wireless sensor network to obtain power from the environment for their entire lifetime. For indoor remote sensors, amorphous silicon photovoltaic (PV) cell can be used to harvest energy from indoor lighting. Furthermore, if the power consumption of the sensor is low, e.g., the image sensor in [1], the power rating of the PV cell can be limited to tens or hundreds of microwatts to minimize the form factor of the sensor. However, as the output power of the PV cell varies greatly with illumination level [2] and the output voltage of the PV cell (V_{PV}), an energy storage device, such as a battery, is required to regulate the harvester's output power. Furthermore, a DC-DC converter with a maximum power point tracker (MPPT) is needed to lock the PV cell at its maximum power point (MPP).

Image sensors usually require a high supply voltage, such as 1.8V in [1], to achieve sufficient sensitivity. However, digital blocks should operate at 1V or less to minimize power consumption. As a result, the remote sensor would require at least 2 power rails to optimize its performance. In [2-4], harvested energy only recharges the battery, thus requiring an additional power converter to deliver energy from the battery to the load. As a result, 2 steps of power conversion are required, which in turn reduces the overall conversion efficiency. In [5], the overall conversion efficiency is improved by delivering the harvested energy to the load and battery in 1 power conversion step.

Figure 4.3.1 shows the architecture of the single-inductor dual-input-tri-output DC-DC buck-boost converter that delivers the harvested energy from the PV cell to the 1V supply (V_{10}), 1.8V supply (V_{18}), or the battery through 1 power conversion step. When the harvested energy is low, power required by the 2 supply rails will be drawn from the battery, which is the 2nd input of the converter. The converter operates in discontinuous conduction mode (DCM) and regulates V_{PV}, V_{18} and V_{10} with a combination of pulse-skipping modulation (PSM) and constant ON time (t_{on}) pulse-frequency modulation (PFM). When the light condition is low and the remote sensor is idling, both the harvested power and load power are very low. As such, the power consumed by the power converter's control circuit has to be reduced to remain efficient. This is achieved by designing the converter to be active only for a short period of time in the entire switching cycle (see Fig. 4.3.2). After the inductor current (I_L) returns to zero (at t_{off}), the converter enters sleep mode and shuts down all its components to reduce power consumption, leaving only the system clock (SYS_CLK) generator in operation. Furthermore, the PSM scheme is utilized so that the dynamic comparators can be employed instead of the error amplifiers and high-speed comparators that have to be in constant operation for PWM and hysteretic control, respectively.
At the beginning of each cycle, the converter is awakened by the rising edge of SYS_CLK. After the Bandgap voltage (V_{BG}) stabilizes, the dynamic comparator (CMP) compares V_{PV}, V_{18} and V_{10} consecutively, with the respective pre-programmed reference voltages generated by the 8b capacitive DAC (CDAC), to determine if the voltages are within their respective ranges. The results are fed to the IN-OUT Selector to determine the input-output pair that will be activated in the current cycle. For example, in Case 1 of Fig. 4.3.2, V_{PV} is above its upper limit, implying that it has excess energy, while V_{10} is below its threshold, which entails that it is low in energy. As such, in this cycle, power is delivered from V_{PV} to V_{10}. In another scenario (see Case 2 of Fig. 4.3.2), all voltages are within their boundaries and no energy transfer is required. As a result, this cycle is *skipped* to reduce power consumption. The measurement results (Fig 4.3.3) show that V_{PV} is switched less frequently than V_{10} and V_{18}, as it was set with a lower current, thus causing it to cross its threshold less often.

To cater for output power covering 4 orders of magnitude, i.e., 1µW to 10mW, PSM alone is ineffective and the frequency of SYS_CLK has to be varied. As shown in Fig. 4.3.1, the SYS_CLK generator comprises of an integrated ring oscillator that generates a 10kHz clock (CLK); a 6b counter that derives other clock frequencies, in octaves, required for PFM; a 2× frequency generator (2X_CLK) to generate a 20kHz clock from the 10kHz clock; and a frequency selector (FREQ_SEL). To reduce power loss, the 2X_CLK is only enabled when the converter needs to operate at 20kHz. The FREQ_SEL determines if the current SYS_CLK frequency needs to be doubled or halved based on the results of the voltage comparison. A simplified flow diagram of the SYS_CLK frequency determining process for V_{18} is as shown in Fig. 4.3.4. Following the flow diagram, the frequency can be doubled whenever 2 consecutive under thresholds are detected. On the other hand, the frequency can be halved when the above threshold is detected for 3 consecutive comparisons. Similar flow diagrams can be drawn for V_{PV} and V_{10}. The SYS_CLK frequency will be doubled when *any* of the voltages requires a doubling of frequency, but it will only be halved when *all* voltages can accept a halving of frequency.

The Perturb and Observe MPPT algorithm is implemented to ensure that the PV cell operates at its MPP [6]. It adjusts the reference voltage setting of V_{PV} ($V_{PV\text{-}REF}$) of the voltage comparator's CDAC. Since indoor lighting conditions are not expected to change rapidly, the MPPT algorithm is implemented with intervals of 3.3s to minimize its power consumption.

The micrograph of the DC-DC converter that is fabricated in a 0.18µm CMOS process and occupies an area of 2.15×2.15mm^2 is shown in Fig. 4.3.7. The measured quiescent power of the converter is 400nW. Due to the low quiescent power, the converter is able to achieve 68% efficiency at an output of 1µW. Due to the dynamic architecture of the converter, lower quiescent power could be achieved by further reducing SYS_CLK's frequency. The converter exhibits a peak efficiency of 83% and maintains an efficiency of more than 65% from 1µW to 10mW. A major cause for the degradation in conversion efficiency is the sub-optimal zero-current detector (ZCD), which results in a significant portion of the input power not being transferred to the output.

The comparison with the state-of-the-art energy harvesters is presented in Fig. 4.3.6. Among the state-of-art harvesters listed in the figure, this work has the lowest power consumption in its control circuit (0.4µW), thus enabling it to achieve the highest conversion efficiency at several microwatts of power. Although [2] has a higher peak efficiency, when the MPPT is excluded, it requires another power converter to interface between the battery and the load. As a result, the expected overall peak conversion efficiency of [2] is expected to be lower than this work. Finally, this work generates a 1.8V supply rail for the sensors and analog circuits, and a 1V supply rail for the digital logic blocks so that the performance and power consumption of the overall remote sensor can be optimized.

Acknowledgements:
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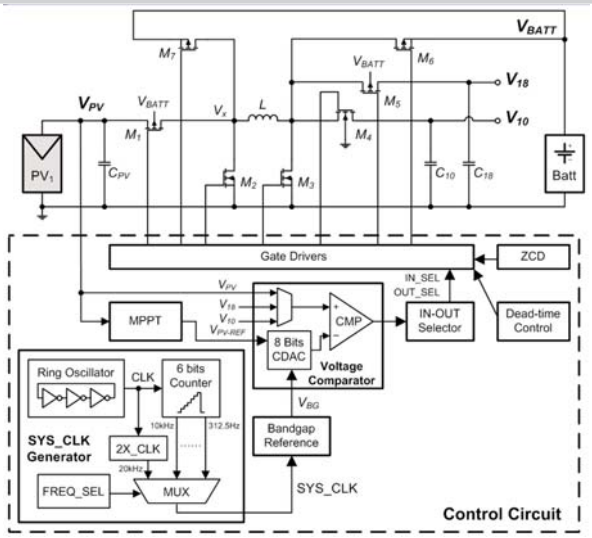

Figure 4.3.1: Block diagram of the single-inductor dual-input-tri-output DC-DC buck-boost converter.

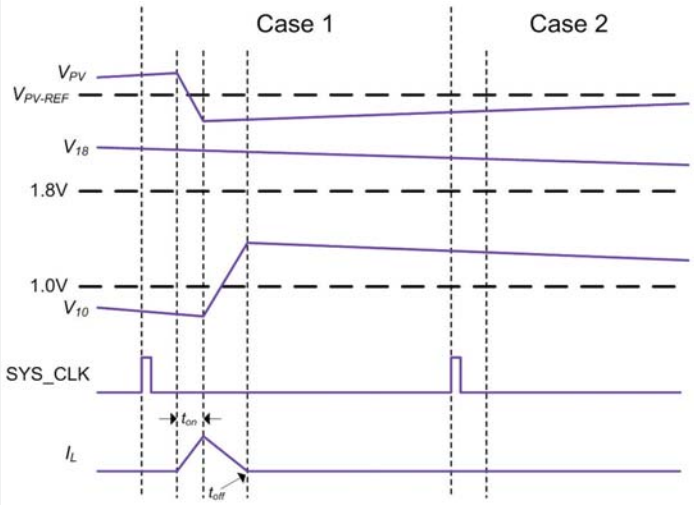

Figure 4.3.2: Operation of the PSM control.

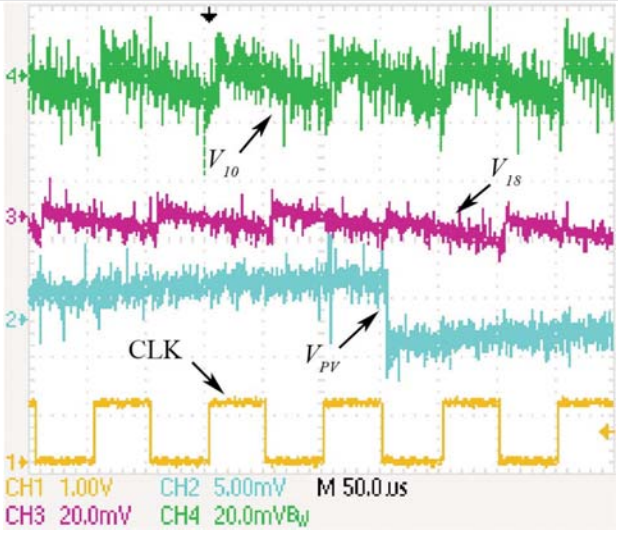

Figure 4.3.3: Measured waveform showing the voltage ripples of V_{PV}, V_{18} and V_{10}.

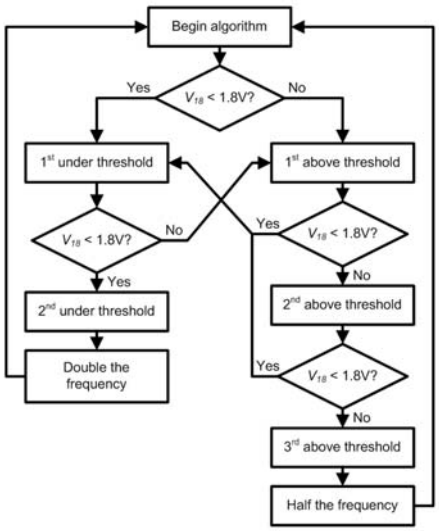

Figure 4.3.4: Flow diagram of V_{18} to determine if SYS_CLK frequency should be doubled or halved.

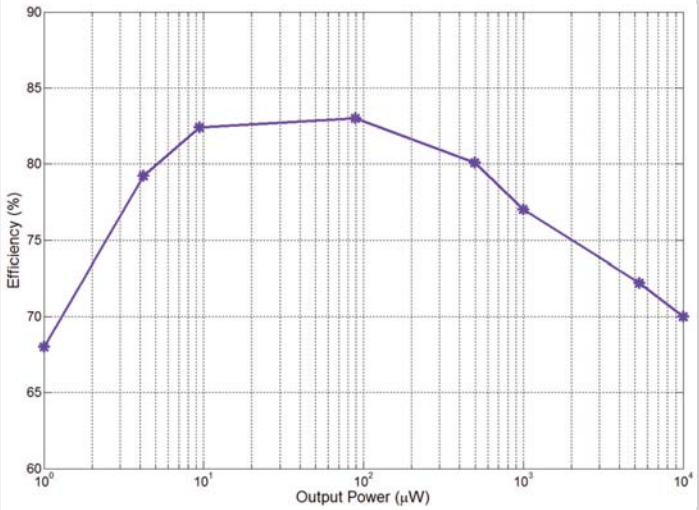

Figure 4.3.5: Measured conversion efficiency under various output power.

	[3]	[4]	[2]	This Work
Output voltage	2V	5.5V	3V	1V, 1.8V and 3V
Output power	10µW to 1mW	621µW	5µW to 10mW	1µW to 10mW
Power consumption of control circuit	2.4µW	135µW	1.95µW	0.4µW
Architecture	Integrated charge pump	Inductive boost converter	Inductive boost converter	Inductive buck-boost converter
Peak conversion efficiency	70%	76%	87% (w/o MPPT) 70% (with MPPT)	83% (with MPPT)

Figure 4.3.6: Comparison of the state-of-the-art energy harvesters.

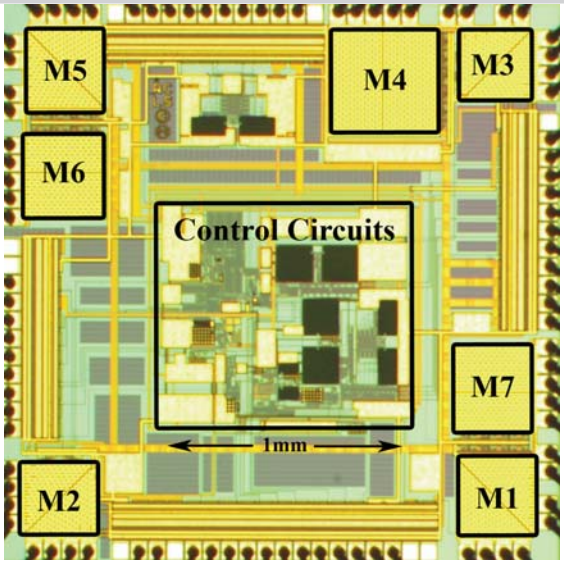

Figure 4.3.7: Micrograph of the converter in 0.18µm CMOS.

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